What is Claimed is:

1. An apparatus for determining gate fall delay for critical path analysis, the apparatus comprising:

a device coupled between a controlling input of a gate and a non-controlling input of the gate,

wherein signals at the controlling and non-controlling inputs rise substantially simultaneously on a first edge; and

on a remaining edge, a signal at the non-controlling input follows a fall of a signal at the controlling input after a fall delay.

2. The apparatus of claim 1 wherein the apparatus provides both rising and falling delays for the critical path analysis of the gate.

3. The apparatus of claim 1 wherein the controlling input is an input of the device.

4. The apparatus of claim 1 wherein the non-controlling input is an output of the device.

5. The apparatus of claim 1 wherein the signals at both the controlling and non-controlling inputs rise on the first edge without any finite delay.

6. The apparatus of claim 1 wherein the device includes at least three VCVS devices coupled between the controlling and non-controlling nodes.

7. The apparatus of claim 6 wherein each VCVS includes:

a positive controlling node (VC+);

a negative controlling node (VC-);

a positive element node (N+); and

a negative element node (N-).

8. The apparatus of claim 7 wherein a plurality of negative controlling nodes (VC-) is grounded.

9. The apparatus of claim 7 wherein at least two of the negative element nodes (N-) are grounded.

10. The apparatus of claim 7 wherein the controlling input is coupled to at least two of the positive controlling nodes (VC+).

11. The apparatus of claim 7 wherein a positive element node (N+) of a first VCVS is provided to a negative element node (N-) of a second VCVS.

12. The apparatus of claim 7 wherein a positive element node (N+) of a first VCVS is provided to a positive controlling node (VC+) of a second VCVS.

13. The apparatus of claim 1 wherein the gate is one selected from a list comprising AND, NAND, OR, NOR, and AOI gates.

14. The apparatus of claim 1 wherein the first edge occurs prior to the remaining edge.

15. An apparatus for determining gate rise delay for critical path analysis, the apparatus comprising:

a device coupled between a controlling input of a gate and a non-controlling input of the gate,

wherein a signal at the non-controlling input follows a rise of a signal at the controlling input after a rise delay on a first edge; and

on a remaining edge, signals at the controlling and non-controlling inputs fall substantially simultaneously.

16. The apparatus of claim 15 wherein the apparatus provides both rising and falling delays for the critical path analysis of the gate.

17. The apparatus of claim 15 wherein the controlling input is an input of the device.

18. The apparatus of claim 15 wherein the non-controlling input is an output of the device.

19. The apparatus of claim 15 wherein the signals at both the controlling and non-controlling inputs fall on the remaining edge without any finite delay.

20. The apparatus of claim 15 wherein the device includes at least three VCVS devices coupled between the controlling and non-controlling nodes.

21. The apparatus of claim 20 wherein each VCVS includes:

a positive controlling node (VC+);

a negative controlling node (VC-);

a positive element node (N+); and

a negative element node (N-).

22. The apparatus of claim 21 wherein a plurality of negative controlling nodes (VC-) is grounded.

23. The apparatus of claim 21 wherein at least two of the negative element nodes (N-) are grounded.

24. The apparatus of claim 21 wherein the controlling input is coupled to at least two of the positive controlling nodes (VC+).

25. The apparatus of claim 21 wherein a positive element node (N+) of a first VCVS is provided to a negative element node (N-) of a second VCVS.

26. The apparatus of claim 21 wherein a positive element node (N+) of a first VCVS is provided to a positive controlling node (VC+) of a second VCVS.

27. The apparatus of claim 15 wherein the gate is one selected from a list comprising AND, NAND, OR, NOR, and AOI gates.

28. The apparatus of claim 15 wherein the first edge occurs prior to the remaining edge.

29. A method of critical path analysis, the method comprising:

providing a device coupled between a controlling input of a gate and a non-controlling input of the gate,

wherein one or more of following (a) or (b) occurs:

(a) signals at the controlling and non-controlling inputs rise substantially simultaneously on a first edge; and on a remaining edge, a signal at the non-controlling input follows a fall of a signal at the controlling input after a fall delay; and

(b) a signal at the non-controlling input follows a rise of a signal at the controlling input after a rise delay on a first edge; and on a remaining edge, signals at the controlling and non-controlling inputs fall substantially simultaneously.

30. The method of claim 29 wherein the device provides both rising and falling delays for the critical path analysis of the gate.

31. The method of claim 29 wherein the controlling input is an input of the device.

32. The method of claim 29 wherein the non-controlling input is an output of the device.

33. An computer program for performing critical path analysis, the computer program comprising:

a machine readable medium that provides instructions that, if executed by a machine, will cause the machine to perform operations including:

providing a device coupled between a controlling input of a gate and a non-controlling input of the gate,

wherein one or more of following (a) or (b) occurs:

(a) signals at the controlling and non-controlling inputs rise substantially simultaneously on a first edge; and on a remaining edge, a signal at the non-controlling input follows a fall of a signal at the controlling input after a fall delay; and

(b) a signal at the non-controlling input follows a rise of a signal at the controlling input after a rise delay on a first edge; and on a remaining edge, signals at the controlling and non-controlling inputs fall substantially simultaneously.

34. The computer program of claim 33 wherein the machine readable medium utilizes an operating system selected from a group comprising Solaris, Windows NT, Windows 2000, Windows XP, Windows ME, HP-UX, Unix, BSD Unix, Linux, and AUX.